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INTERFACE PROPERTIES AND SURFACE LEAKAGE OF HGCDTE PHOTODIODES.(U)
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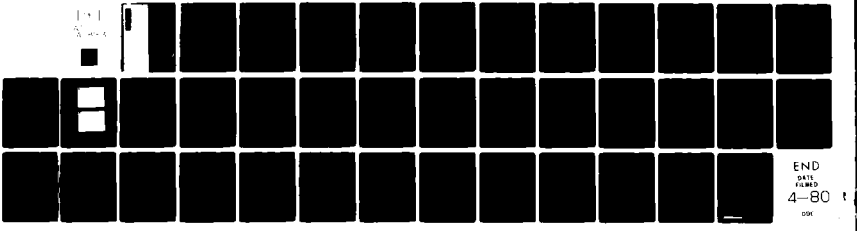

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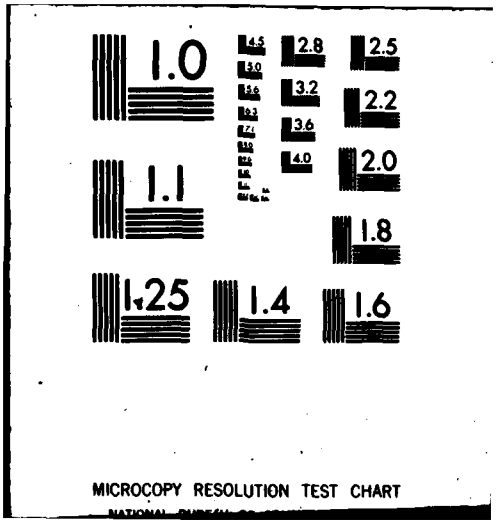
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Technical Report 80-3c

INTERFACE PROPERTIES AND SURFACE LEAKAGE OF (Hg,Cd)Te PHOTODIODES

Interim Report

by:

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ABSTRACT

A program was undertaken to determine the origin of surface leakage associated with $Hg_{1-x}Cd_xTe$ photodiodes and to seek improved surface passivation techniques. To attain this goal, emphasis was placed on surface spectroscopic analyses and metal-insulator-semiconductor (MIS) characterizations of candidate passivants.

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During the initial four months of the program, the insulating and interfacial properties of anodic oxides and ZnS on $Hg_{0.8}Cd_{0.2}Te$ were investigated. X-ray photoelectron spectroscopy (XPS) techniques were developed for determining depth profiles of compositional variations in the semiconductor with a minimum materials damage. Using these techniques, we found that (a) the composition of a 1200 Å anodic film is 68% TeO_2, 27% CdO, and 6% HgO, and (b) the cations, especially the Hg ions in the semiconductor, are significantly depleted near the interface. The capacitance-voltage curves from MIS measurements of the same specimen exhibited a large hysteresis and a characteristic indicative of a high density of surface states. A tentative interpretation for these results is that dissociation of the chemically unstable HgO into Hg^{+2} and O^{-2} in the oxide is responsible for the hysteresis, while the cation vacancies in the semiconductor create defect states near the interface. Also, we have found a strong interaction between deposited ZnS layers and $Hg_{0.8}Cd_{0.2}Te$ resulting in the formation of an interfacial layer of $ZnS_{1-y}Te_y$.

The consequence of these chemical and electrical properties to diode passivation is discussed.

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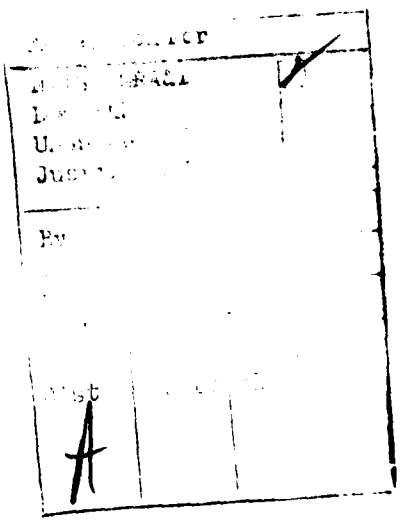

FIGURES

1. INTRODUCTION

The alloy system $Hg_{1-x}Cd_xTe$ ((Hg,Cd)Te) has great potential for broad application in the field of infrared detection. The band gap and long wavelength cutoff of the alloy can be adjusted from 0 to 1.6 eV (0.77 μm or longer) by varying the alloy composition, thus making it suitable as an intrinsic detector for most of the infrared spectrum.

The performances of good quality (Hg,Cd)Te photodiodes have been discussed in a number of recent publications.[1-4] The general consensus is that a major limitation to the ultimate performance of these diodes arises from surface leakage, which can be attributed to four primary mechanisms: (a) surface generation-recombination states, (b) bulk generation-recombination states within the surface depletion region, (c) diffusion of minority carriers to the surface depletion region, and (d) material defects that shunt the surface junction. In general, these problems can be solved or minimized by properly passivating the device surface. Accordingly, surface passivation becomes an extremely important step in the fabrication of high performance (Hg,Cd)Te devices.

A good passivant should possess the following features: (a) low surface state density, (b) tailorable surface potential, (c) minimum insulator trap density and fixed charges, (d) stability with respect to a wide range of temperature, ambient gases, and light irradiation, and (e) stability against device processing and handling. Thus, the criteria for a good passivant is not only concerned with the intrinsic properties of the passivant, but also the interfacial properties

of the passivated (Hg,Cd)Te. The latter are controlled by the interactions between the passivant and the (Hg,Cd)Te surface, and hence are dependent on how the passivant is fabricated on (Hg,Cd)Te.

Compared with the surfaces of other semiconductor (e.g. Si, GaAs, etc.) the surface of (Hg,Cd)Te is particulary sensitive to chemical and physical treatments. This sensitivity was revealed in a company supported study of this material using surface analytical spectroscopies, where we have found that (a) the standard etching process using bromine in methanol can cause depletion of cations and produce a surface layer of TeO_2 (Fig. 1); (b) irradiation with an electron beam of a few keV energy can convert the surface layer (10-100 Å) of (Hg,Cd)Te into CdTe (Fig. 2); and (c) sputtering with Ar ions of 1-2 keV energy can cause the chemical composition of the top monolayer to change (to be discussed in 2.3.2). Because of the activity of the (Hg,Cd)Te surface, a strong (Hg,Cd)Te/passivant interaction is expected. Therefore, any viable approach toward attaining improved passivants must consider the nature of this interaction and its effect on the electrical properties of the insulator.

Therefore, in view of the importance of surface passivation for the (Hg,Cd)Te technology, we have initiated, under this contract, a study of the properties of two candidate passivants, native oxide and ZnS, on $Hg_{0.8}Cd_{0.2}Te$. The objective is to determine the origin of surface leakage associated with $Hg_{0.8}Cd_{0.2}Te$ photodiodes and to seek improved surface passivation techniques.

To attain this goal, we have placed an emphasis of our research technique on surface analysis and metal-insulator-semiconductor (MIS) capacitor characterization.

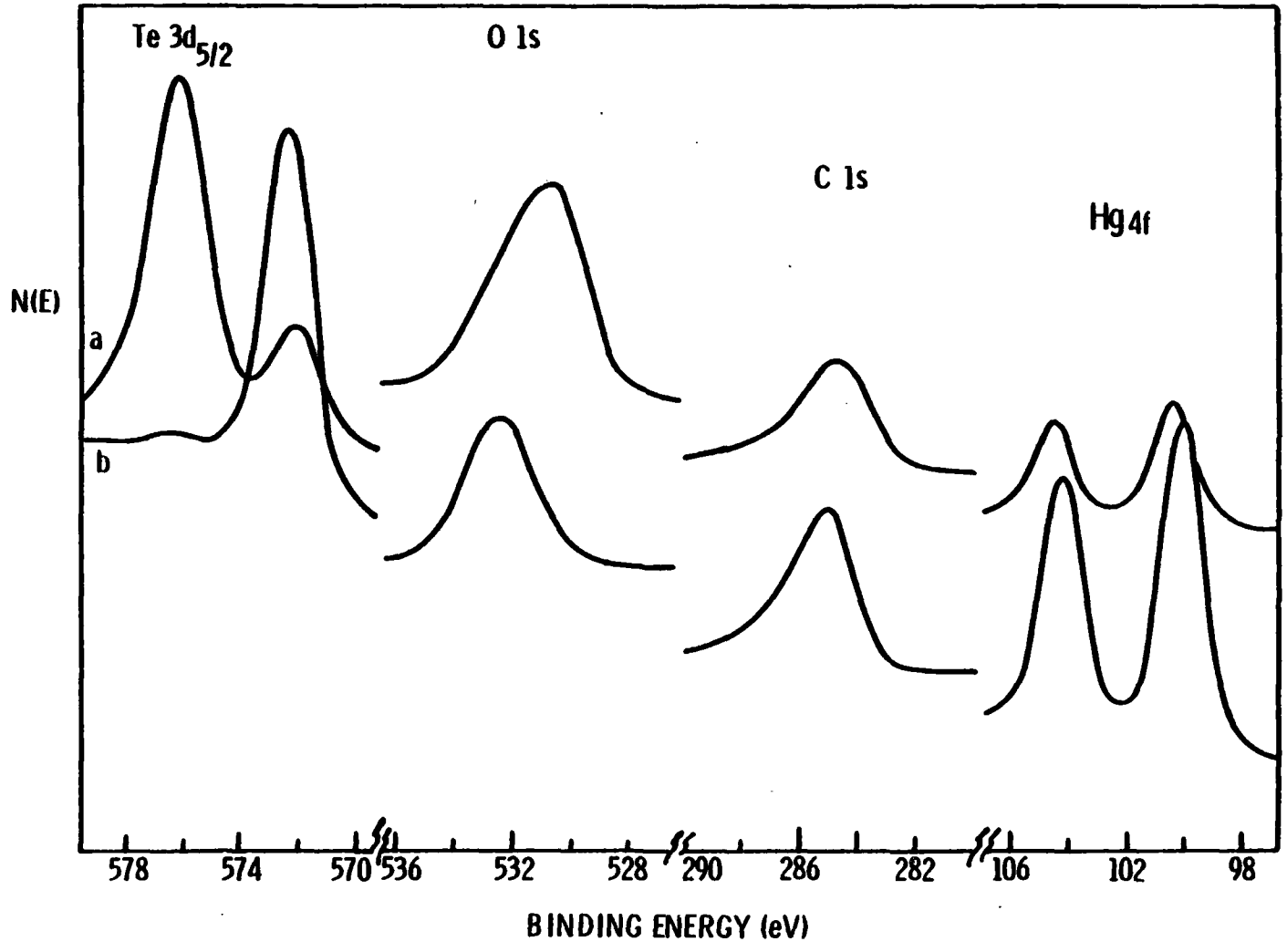

Figure 1. XPS spectra of $Hg_{0.8}Cd_{0.2}Te$ surfaces, a) etched with bromine in methanol, and b) mechanically polished.

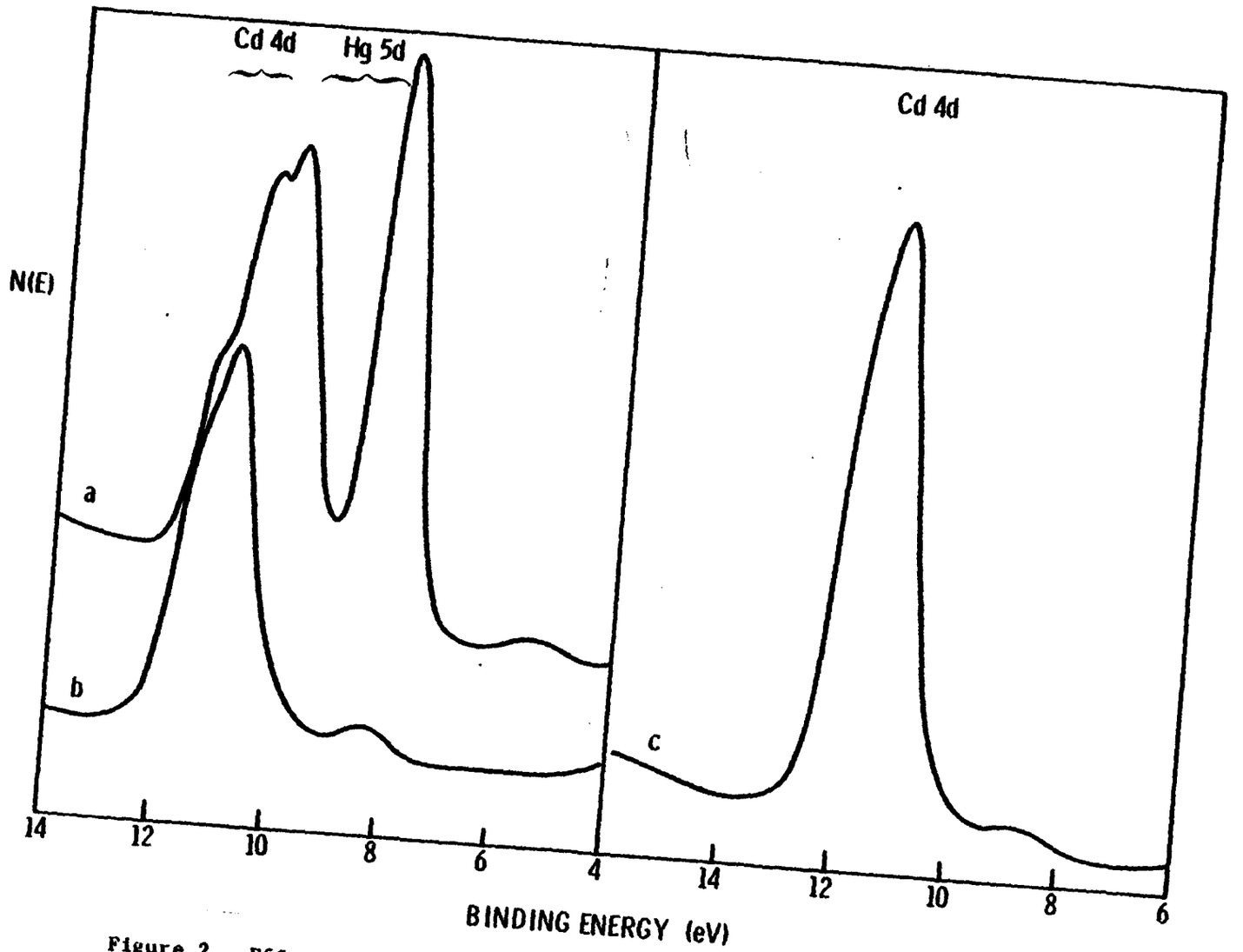

Figure 2. Effect of electron-beam irradiation of $Hg_{0.8}Cd_{0.2}Te$ surfaces revealed by UV photoelectron spectroscopy (UPS). The Hg 5d structure observed in the spectrum for the un-irradiated surface (a) vanishes after a 1 minute irradiation with a 2 keV electron beam, resulting in a spectrum (b) comparable with that for a CdTe surface (c).

Surface analysis involves the use of Auger electron spectroscopy (AES), x-ray photoelectron spectroscopy (XPS) and uv photoelectron spectroscopy (UPS). These spectroscopies were chosen on the basis of their surface sensitivity, their chemical analytical ability and their applicability in depth composition profiling, so that the chemical properties of the passivant and of the interface between the passivant and (Hg,Cd)Te can be studied in great detail. These capabilities were successfully exploited in the studies of a number of semiconductors (e.g. SiO_2/Si and (native oxide, metal)/GaAs)[5] resulting in unprecedented progress in the Si and GaAs technologies. It is anticipated that a great deal of new knowledge concerning (Hg,Cd)Te can be learned from similar surface studies.

The electrical characteristics of an MIS device can provide useful information about the electronic properties of the insulator/semiconductor interface region. By fabricating an MIS device with the passivant as the insulator, we can determine the surface states density, surface potential, surface recombination velocity, and minority carrier lifetime, all of which are essential parameters controlling surface leakage. Thus, by combining such measurements with the surface spectroscopic analyses, the physical origins of surface leakage can be properly located, and the problem of surface leakage can be studied in great depth.

In this interim report, we summarize the work that has been done on the program in the period August 30, 1979 to January 20, 1980. The details of the experimental techniques are discussed in Section 2, and the experimental results in Section 3. A conclusion and some recommendations for future work based on our findings are given in Section 4.

2. EXPERIMENTAL TECHNIQUES

2.1 MIS Capacitor Fabrication

2.1.1 $Hg_{0.8}Cd_{0.2}Te$ substrate preparation

All the HgCdTe wafers (15 mm diameter and 1 mm thick) were supplied by Cominco American, Inc. After removing a wafer from the container in which it was shipped, the wafer was washed in trichlorethylene and mounted on a macor disk using crystal bond heated to 100°C. The wafers were subsequently polished on a very soft polishing cloth (Buehler AB Selvyt No. 40-7008) using Buehler Metpolish Chromic Oxide #2 with a particle size of 0.5 μm. Once a flat surface was obtained it was thoroughly washed in water, then rinsed in methanol prior to being chemically lapped on another soft polishing cloth (same as for mechanical polishing) to remove the scratches. The polishing cloth was secured to a glass polishing disk which is not affected by the corrosive nature of the etch — a 5% solution of bromine in methanol. A thorough rinse in methanol completed the chemical lapping step.

A major problem we have encountered in our work is that arising from etch pits in the $Hg_{0.8}Cd_{0.2}Te$. These etch pits are present in all as-received, polished and etched material purchased from the supplier regardless of whether it is their low grade material purchased in order to develop and familiarize ourselves with the necessary processing procedures, or the high quality material intended for in-depth studies of passivating film performance. These pits are due to both inclusions and voids in the $Hg_{0.8}Cd_{0.2}Te$ and apparently are formed during the growth of the material. The voids can be seen in material which has just been mechanically polished, whereas the inclusions, consisting most likely of Hg, are revealed during the etching process because they give rise to preferential etching. It was observed that many etch pits appear

along lines suggesting that the inclusions are preferentially formed along dislocation lines in the semiconductor.

The etch pits cause problems in that they act as sites for enhanced dissolution during anodic growth and so result in films with holes in them as shown in Fig. 3. In addition, for the case of ZnS deposited on surfaces containing etch pits, the holes are only covered in the ZnS is thicker than 3000 Å. Such a non-uniform film is not likely to have the most desirable passivating properties, as the induced surface potential will be a function of position on the surface. These defects increase the difficulty of making good MIS devices because the breakdown voltage of the insulator at the defect site is reduced.

In spite of these problems encountered with etch pits, we obtained a measure of success in fabricating MIS devices as long as the anodic film was greater than 1000 Å and the ZnS was greater than 3000 Å.

2.1.2 Insulator Layer Growth

2.1.2.1 Anodization. The anodic oxides were formed using a Texas Instrument patented process[6], which involves the use of 0.01 N KOH in ethylene glycol as electrolyte. During anodization, the current density was kept constant at 0.3 mA/cm^2 and the voltage allowed to increase with time. The thickness of the anodic film is proportional to the applied voltage and therefore can be controlled by the final voltage. The thickness can also be determined from the color of the film[6]. To avoid electric breakdown during MIS capacitance measurement, films thicker than 1000 Å were required. However, for the purpose of reliable surface analysis, the oxide films had to be kept as thin as possible. As a compromise, a thickness of 1200 Å was chosen. In the final step of anodization, the films were rinsed thoroughly in methanol.

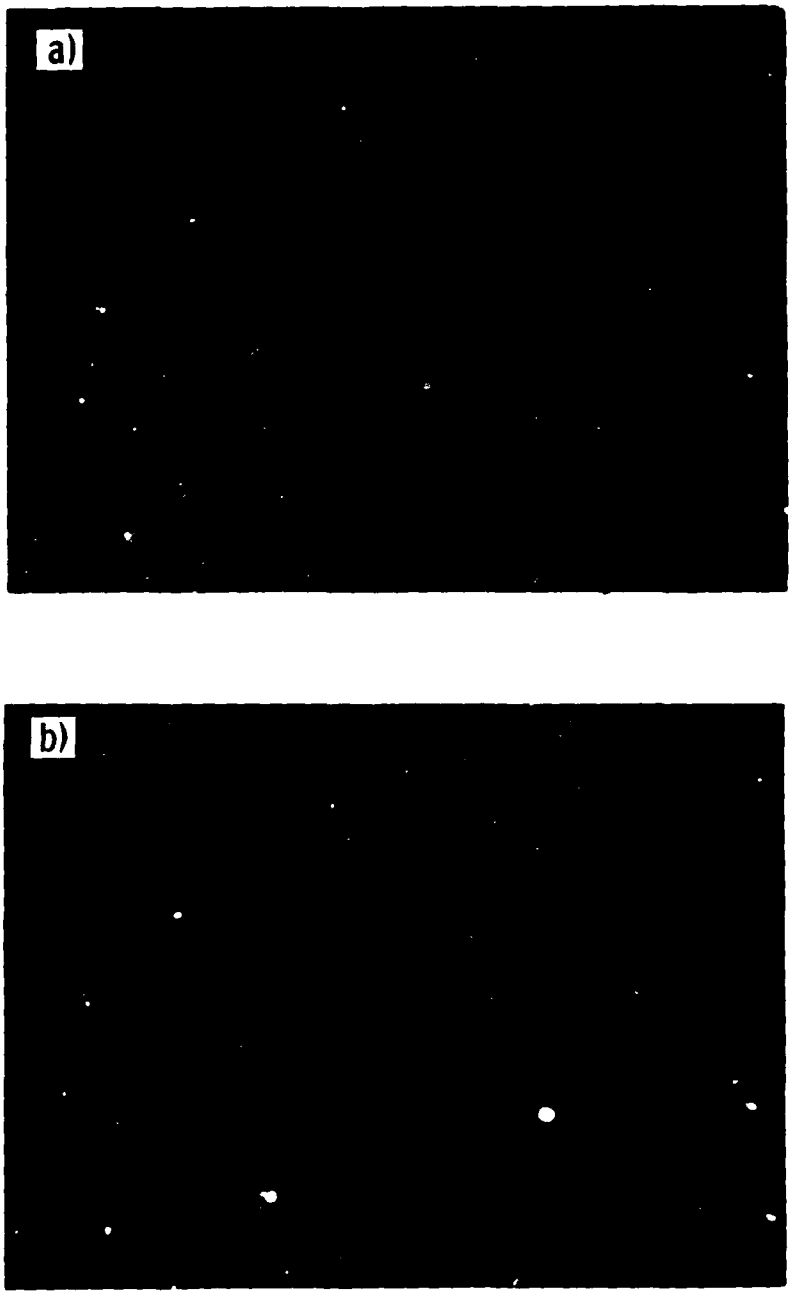

Figure 3. Micrograph (130x) of a) the bare surface of a $Hg_{0.8}Cd_{0.2}Te$ wafer polished and etched as described in Section 2.1.1 and b) the same region of the wafer after anodizing to a thickness of approximately 1,200 Å.

2.1.2.2 ZnS deposition. Three different techniques of growing ZnS films were studied: (1) electron beam evaporation, (2) resistance heating (Knudsen cell), and (3) argon sputtering. The ZnS was deposited on wafers of $Hg_{0.8}Cd_{0.2}Te$ which had been prepared as described in section 2.1.1. The source material in all three cases was sintered ZnS. These methods produced ZnS films of good uniformity and good adhesion to the substrate; and if the films were thicker than 3000 Å, most of the etch pits associated with the inclusions were covered, thereby avoiding pinholes in the insulator.

2.1.3 Ohmic Contact and Field Plate

Gold pads with an area of 0.5 mm^2 and about 1,000 Å thick were evaporated on the insulating film through a metal mask and gold wires 0.025 mm in diameter were attached to the gold pads with epoxy. Initially, conducting gold epoxy was used but the gold epoxy required curing at 100°C for 2 hours and this modified the electrical properties of the MIS device. A two-compound silver epoxy which cures at room temperature is now used to avoid the problems arising from curing at higher temperatures. Ohmic contact to the semiconductor was made with a drop of molten indium placed on an edge containing no passivant.

2.2 C-V and G-V measurements

The electrical properties of the passivant are determined by fabricating an MIS device incorporating the passivant as the insulator and measuring the capacitance and the a.c. conductance as a function of voltage bias applied across the device.

A lock-in amplifier is used both to provide the a.c. modulation signal and to measure the response of the MIS device. By superimposing a ramp voltage with the a.c. signal and applying it to the device, the in-phase and out-of-phase components of the a.c. current can be measured to determine the

capacitance and conductance respectively as a function of the applied bias. The measurements are mostly carried out with the sample in a dewar which can be cooled to 77K and, which provides ample shielding against pick-up of extraneous noise signals. Room temperature measurements are frequently carried out by using probes to make electrical contact to the device, thereby avoiding the use of epoxy altogether.

2.3 Surface Analysis

2.3.1 Technical Problems

The surface analyses were performed with a Physical Electronics spectrometer (Model 548), which is capable of executing Auger electron spectroscopy (AES), x-ray photoelectron spectroscopy (XPS) and uv photoelectron spectroscopy (UPS). The major features of these spectrocopies are shown in Table I. The spectrometer is also equipped with a 2 keV Ar ion sputtering gun for the execution of depth composition profiling and surface cleaning prior to analysis.

TABLE I

Surface Analytical Techniques Available at Martin Marietta Laboratories

Technique	Incident Probe	Sampling Depth	Physical Properties Analyzed
AES (Auger Electron	Electron (1-5 keV)	10-20 Å	• Surface composition (semi-quantitative) • Depth composition profile • Chemical states (limited)
UPS (UV Photoelectron Spectroscopy)	UV Light (21 and 41 eV)	10 Å	• Valance band structure • Surface states (conditioned)
XPS (X-Ray Photoelectron Spectroscopy)	X-Ray (1,250 eV)	10-20 Å	• Surface composition (quantitative) • Chemical states • Depth composition profile (limited)

Two technical problems are encountered in the analysis of (Hg,Cd)Te surfaces. First, argon sputtering leaves (Hg,Cd)Te with a disordered surface which cannot be annealed in vacuo without depleting Hg from the specimen. In general, the damage caused by sputtering is predominant in the top most monolayer (5-10 Å) of the surface. Although it is not critically detrimental to the AES and XPS measurements, the damage creates an electronic structure of its own which can alter the surface state characteristics and thus eliminate the utility of UPS for surface state analysis. Secondly, irradiation by the AES electron beam can convert the surface (10 to 100 Å deep depending on the electron energy) of (Hg,Cd)Te into a layer of CdTe (see Fig. 2). As a consequence, the AES technique is not suitable for probing the surface of (Hg,Cd)Te. However, it can still be applied to the depth profiling of ZnS and the anodic oxide layer. Compared to XPS, the AES technique permits simultaneous measurement and sputtering to produce a continuous, real-time compositional profile. This feature allows one to precisely locate the onset of the insulator semiconductor interface, where the analysis can be performed by XPS.

The XPS technique is not destructive, and because its probing depth is greater than the damaged layer, its susceptibility to the sputtering effect is not critical. With a careful characterization of the sputtering effect, we can make the XPS technique a very reliable and informative tool for the study of (Hg,Cd)Te surfaces. Another important advantage of this technique is that the chemical states of Te (e.g., Te^{-2}, Te, and Te^{+4}) can be unambiguously determined. This feature is particularly important for characterizing (Hg,Cd)Te specimens involved in chemical treatments such as etching and anodization processes.

Accordingly, the XPS technique has been chosen as the primary tool for surface analysis, and the AES technique as an auxiliary, mainly for the depth profiles of insulator layers. However, there are two technical drawbacks in using XPS for depth profiling. (1) The XPS measurement cannot be performed during sputtering, because of the presence of Ar ($5x10^{-5}$ torr pressure) and the high voltage (10 kV) used in the x-ray generator. Nevertheless, discrete-point XPS depth profiles can be obtained by alternating the sputtering process and the XPS measurement consecutively. (2) The area sampled by the XPS is about 25% of the size of the crater ($\sim$20 mm^2) created by sputtering and therefore the surface must possess some degrees of curvature which can cause degradation to the depth resolution of the XPS depth profile.

2.3.2 Calibration of XPS

In order to make a reliable quantitative analysis, it is necessary to precalibrate the intensities of the principal XPS lines. High purity CdO and TeO_2 powders, sintered ZnS pellets, single-crystals and polycrystals of $Hg_{1-x}Cd_xTe$ (x = 0.2, 0.3 and 1.0) and their anodic films, were used as references for calibration. The measured sensitivity factors for six major XPS lines are shown in Table II.

TABLE II

Sensitivity Factors and Binding Energies of XPS Lines in $Hg_{1-x}Cd_xTe$

XPS Line		O1s	$Hg4f_{7/2}$	$Cd3d_{5/2}$	$Te3d_{5/2}$	$Zn2p_{3/2}$	S2p
Binding energy (eV)		530.3	100.4	404.8	572.5(576.0)	1022.0	161.5
Sensitivity Factor	a-	0.45	2.19	2.30	4.0[b]	5.3[b]	0.36
	b-	0.63	2.1	2.55	4.0	5.3	0.35

a- this work; b- from reference 7.

Except for the O1s line, our sensitivity factors agree with the published value[7] within 7%. The discrepancy in the two O1s sensitivity factors is probably due to a strong dependence of the O 1s intensity on the bonding nature of the oxide.

Based on the above result, we were able to estimate that Ar sputtering caused a 22% depletion of Hg on $Hg_{1-x}Cd_xTe$ surfaces and a 14% reduction of TeO_2 on oxide surfaces. These figures suggest that the damage caused by 2 keV Ar ion bombardment is predominantly confined to the topmost monolayer of the solid.

3. EXPERIMENTAL RESULT

3.1 Anodic Oxide on $Hg_{0.8}Cd_{0.2}Te$

3.1.1 MIS Measurements

The results of capacitance-voltage (C-V) measurements on MIS capacitors with 1200 Å anodic oxide insulators are shown in Fig. 4. From the curve we have obtained the following qualitative information:

(1) The surface potential can be biased all the way from accumulation to inversion and at zero applied bias is accumulated.

(2) There is a high density of surface states across the entire band gap which manifests itself partly as a shoulder on the curve.

(3) The number of trapped charges in the oxide is quite sizeable as evidenced by the large hysteresis in the curve when the direction of the voltage ramp is reversed.

(4) The minority carriers are able to follow the a.c. signal which has a frequency of 100 kHz. This implies that the minority carrier lifetime is very short (<1 ns).

No attempt to fit a theoretical curve to the experimental one was made because of the large number of surface states and trapped charges that are obviously present.

3.1.2 Surface Analysis

An XPS depth composition profile (Fig. 5) was performed on a $Hg_{0.8}Cd_{0.2}Te$ specimen with the anodic film used in the MIS capacitors. Except for the surface region where composition is complicated by the

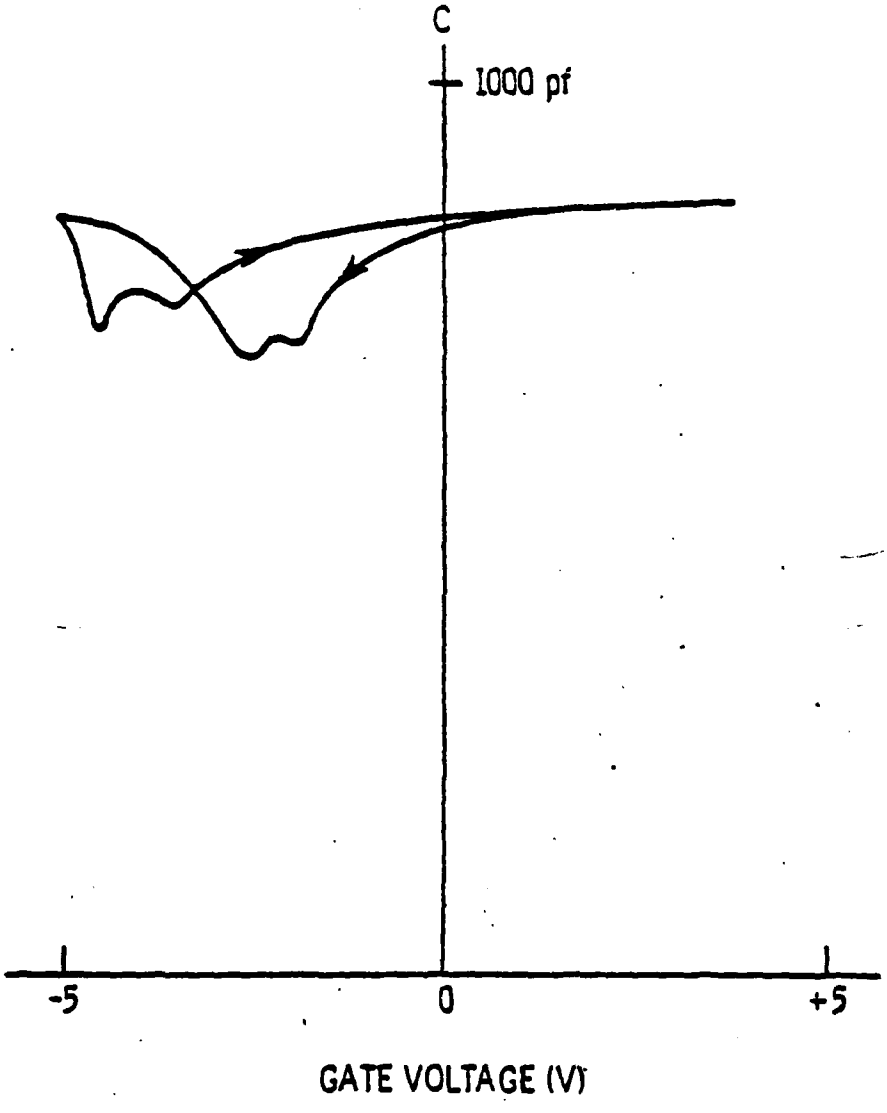

Figure 4. C-V curve for anodic oxide on p-type ($p \approx 10^{17}$ cm^{-3}) $Hg_{0.8}Cd_{0.2}Te$ measured at 77K at a frequency of 100 kHz.

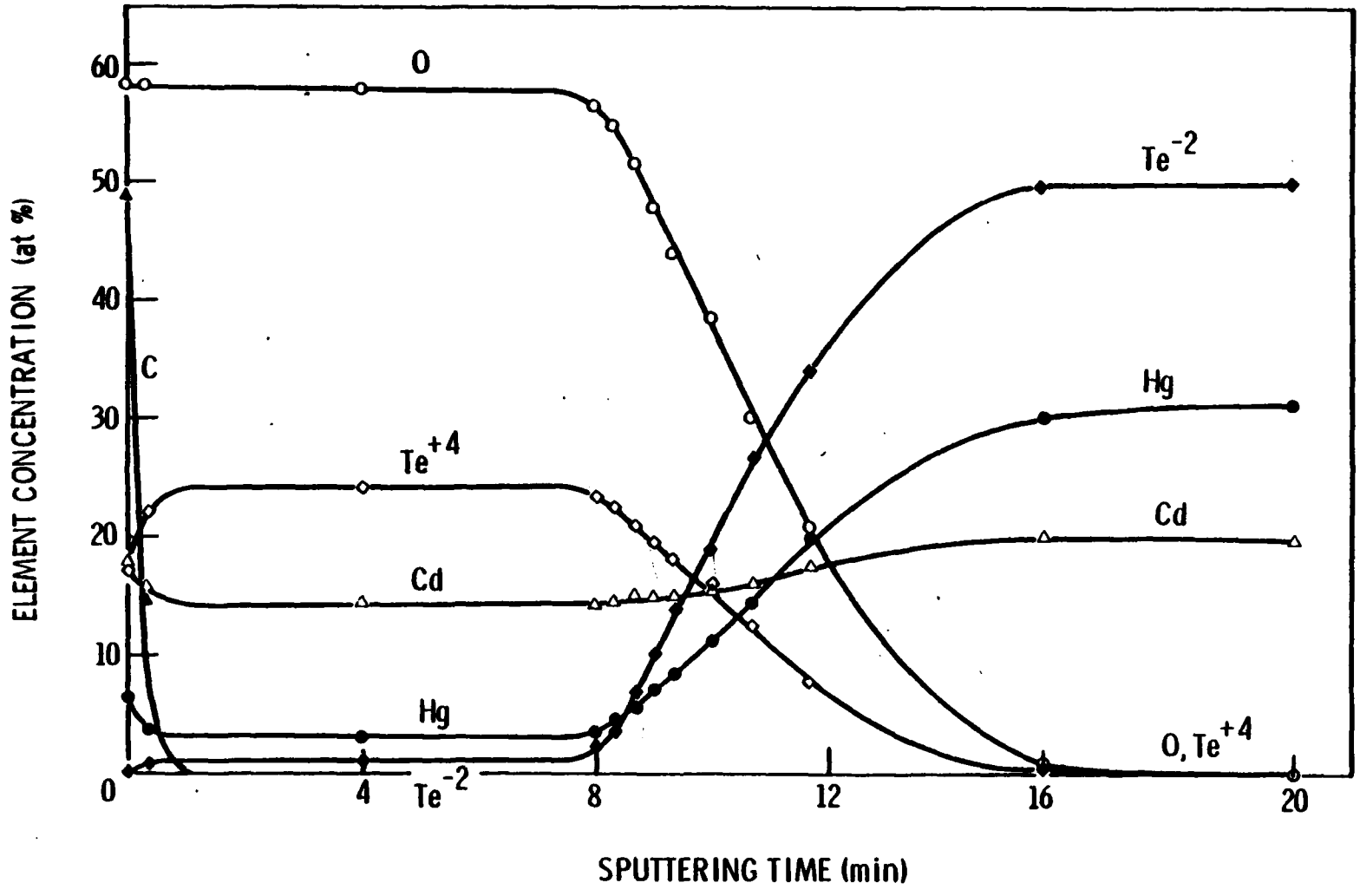

Figure 5. The XPS depth composition profile of an anodized $Hg_{0.8}Cd_{0.2}Te$ specimen. The oxide thickness is 1200 Å, determined by anodizing voltage.

presence of hydrocarbon contaminant, the oxide composition appears to be very uniform over the entire thickness. The elemental composition of the oxide is 58% O, 24% Te, 14% Cd and 3% Hg. A chemical state analysis of these elements based on their binding energies suggests that the anodic layer is a compound of 68% TeO_2, 27% CdO and 6% HgO. Previously Nemirovsky and Finkman[8] studied the optical properties of the anodic oxides of $Hg_{0.8}Cd_{0.2}Te$ and concluded that the predominant constituent of the anodic oxide is TeO_2. However, their result revealed no evidence of CdO. We believe that the refractive index data in their study were not complete enough for an unambiguous composition analysis, therefore their conclusion about the absence of CdO is suspect.

The broad transition region between 8 and 16 min on the sputtering time axis in Fig. 5, is not evidence of a diffuse oxide/semiconductor interface, but rather indicates the effect of degraded depth resolution due to surface microroughness[9] and the surface curvature induced by the sputtering process. If it were due to a diffuse interface, the oxygen stoichiometry would change gradually with depth and there would be an intermediate chemical state for the Te ions to change from the cation state (Te^{+4}) to the anion state (Te^{-2}). However, each XPS spectrum in the transition region of Fig. 5 shows only two $Te3d_{5/2}$ peaks, Te^{+4} (576.0 eV) and Te^{-2} (572.5 eV), i.e., the transition from a pure oxide spectrum to a pure semiconductor spectrum involves only changes in the relative intensities of these two peaks but not changes in their binding energies. Therefore, we believe that the interface has a microscopically small width.

In order to analyze the composition of the semiconductor at the interface, the oxide contribution must be separated from the XPS data in the oxide/semiconductor transition region. Our approach (see Appendix) is to

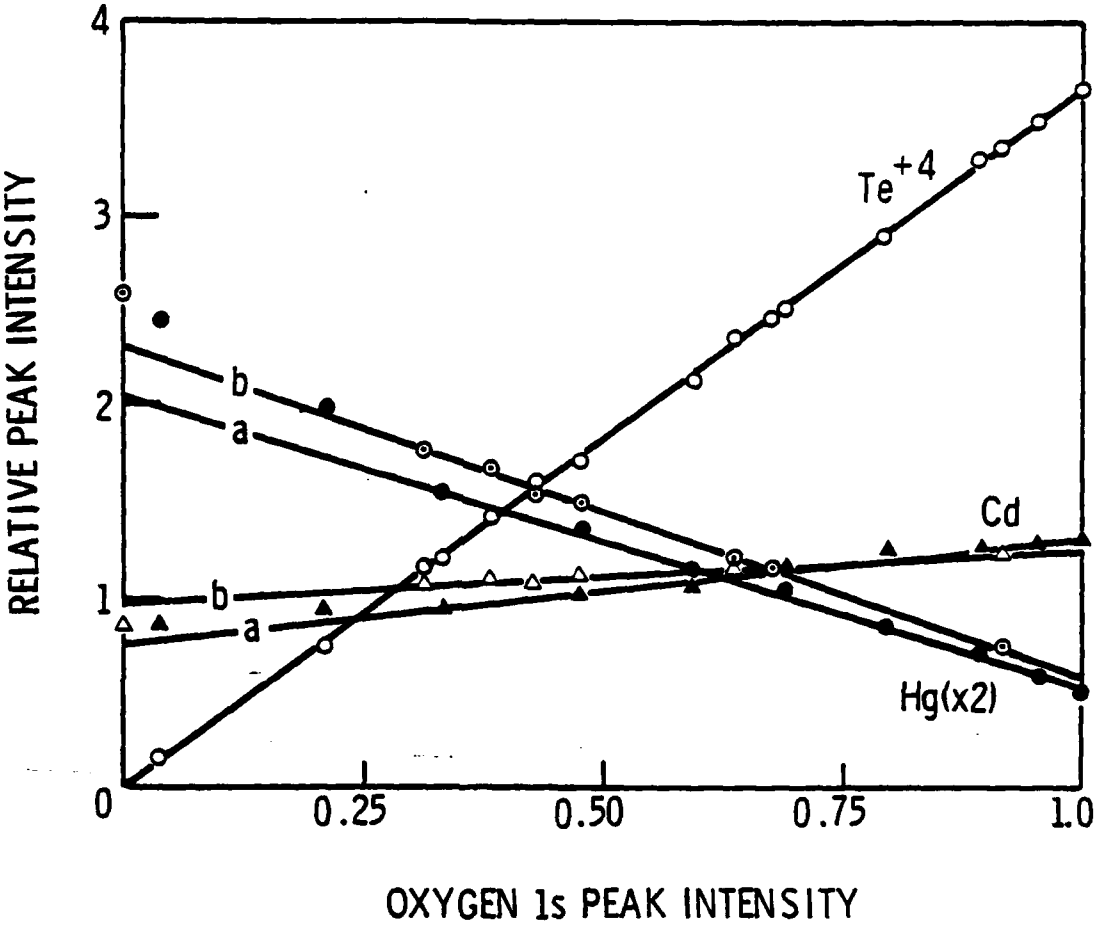

Figure 6. Relative peak intensities of Te^{+4} $3d_{5/2}$, Cd $3d_{5/2}$ and Hg $4f_{7/2}$ versus O 1s peak intensity. ● and ▲ represent data obtained during depth profiling with sample position fixed. ⊙ and △ represent data obtained at the end of 20 min sputtering by moving the sample laterally with respect to the analyzer.

plot the XPS peak intensity of each constituent as a function of the oxygen intensity as shown in Fig. 6. The intensity of Te^{+4} species is linearly proportional to the oxygen intensity, indicating the invariance of oxide stoichiometry with depth. Both Hg4f and Cd3d have small chemical shifts from the oxide state to the telluride state; therefore their intensity contains both oxide and telluride components. However, by extrapolating the line, which best fits the data points at high oxygen intensities, to intersect the axis of zero oxygen intensity, we can determine the concentration of non-oxide components of Hg and Cd near the interface region (see Appendix). The result (line (a) of Fig. 6) shows that the composition of semiconductor at the interface is 54.4% Te, 27.3% Hg and 18.3% Cd, as compared to 49.8% Te, 30.7% Hg, and 19.5% Cd measured in the bulk (Fig. 5). Thus, in the vicinity of the interface, Hg is depleted by 12% and Cd by 6% with respect to Te. This result does not support the model proposed by Nemirosky and Finkman[8] involving a Hg build-up at the interface. Note that three measurements on the left-hand side of Fig. 6, which are performed after 12, 16 and 20 min of sputtering (see Fig. 5), show a higher intensity of Hg than the average intensity of interfacial Hg (represented by line a). From this data, we estimate an upper bound for the depth of the cation-depleted region to be about 400 Å (based on the sputtering rate for the oxide).

The phenomenon of cation depletion at the interface has also been observed in oxidized GaAs involving plasma, thermal and anodic oxidation techniques[10,11]. Chang, et al[10] studied the plasma-grown oxide on GaAs using AES depth profiling technique and showed that excess As in an elemental state builds up at the oxide/GaAs interface. They attributed the depletion of Ga at the interface to preferential oxidation of Ga due to the higher heat of formation of Ga_2O_3 compared to As_2O_3. We believe that, in the

case of $Hg_{1-x}Cd_2Te$, preferential dissolution of Hg in the electrolyte and preferential oxidation of Cd with respect to Te under the assistance of an electric field, are responsible for depletion of both cations in the interface region. The second mechanism is substantiated by the fact that the ratio Cd/Te in the anodic film is 0.58, almost three times the x value. However, based on the chemical-shift analysis of the Te $3d_{5/2}$ peak, we do not find evidence of elemental (or covalent) Te formed in the interface region. Therefore, we believe that this region is highly disordered, having a high concentration of cation vacancies but no precipitates of Te.

The results from the surface analysis of the oxide and interface compositions have two important implications. Firstly, the oxide is a heterogeneous compound and in particular, contains 6% HgO which is not chemically stable. The free energy of formation for HgO is 14 kCal/mole, much smaller than the values for most oxides (e.g., 54, 64, and 196 kCal/mole for CdO, TeO_2, and SiO_2, respectively) and consequently HgO can readily decompose into Hg and O_2 by thermal heating, light irradiation and electric field. We believe that the presence of HgO may provide trapped and fixed charges in the anodic oxide of (Hg,Cd)Te via $HgO \rightarrow Hg^{+2} + O_2^{-2}$ process. Evidence of trapped charges in the anodic film has been confirmed by a large hysteresis in the C-V curves of an MIS capacitor made from the same specimen (3.1.1). Secondly, the substantial depletion of cations leads to defects in the interface region, which possibly are electrically active. As a consequence, a high density of surface states and generation-recombination centers are present in the interface region, causing increased surface leakage. This conclusion is also substantiated by the C-V measurements from the same specimen.

3.1.3 Effects of Heat Treatment

Experiments were performed to study the effects of heat treatment (110°C for 2 hours in air) on the anodic films of $Hg_{0.8}Cd_{0.2}Te$. No apparent effect has been observed on the chemical composition in both oxide and interface regions. However, the MIS measurement (Fig. 7) revealed the following effects:

(1) An increase in the a.c. conductivity which implies an increase in the surface state density.

(2) A shift of about 1 volt in the flat band potential due to charges trapped in the oxide

(3) A large increase in the hysteresis also associated with trapped charges in the oxide.

It should also be noted that the conductance in inversion does not change very much upon heating but that the dielectric loss tangent for this voltage region is quite large ($\tan^{-1}\left(\frac{G}{\omega C}\right) = 0.3$) implying a lossy film.

Visible light had no discernible effect on the C-V or G-V curves.

3.2 ZnS Deposited on $Hg_{0.8}Cd_{0.2}Te$

3.2.1 Surface Analysis

A depth composition profile was performed on a 500 Å ZnS film deposited by the electron beam method on $Hd_{0.8}Cd_{0.2}Te$ (Fig. 8), using both XPS and AES. The AES was used only in the ZnS layer. Both AES and XPS data showed that the upper half (∿300 Å) of the ZnS film had a uniform composition of $ZnS_{1-y}Te_y$, with increasing y value toward the ZnS/(Hg,Cd)Te interface. Since S and Te are isoelectronic, it is possible that during ZnS deposition, Te^{-2} ions diffuse into the ZnS layer and substitute for S^{-2}

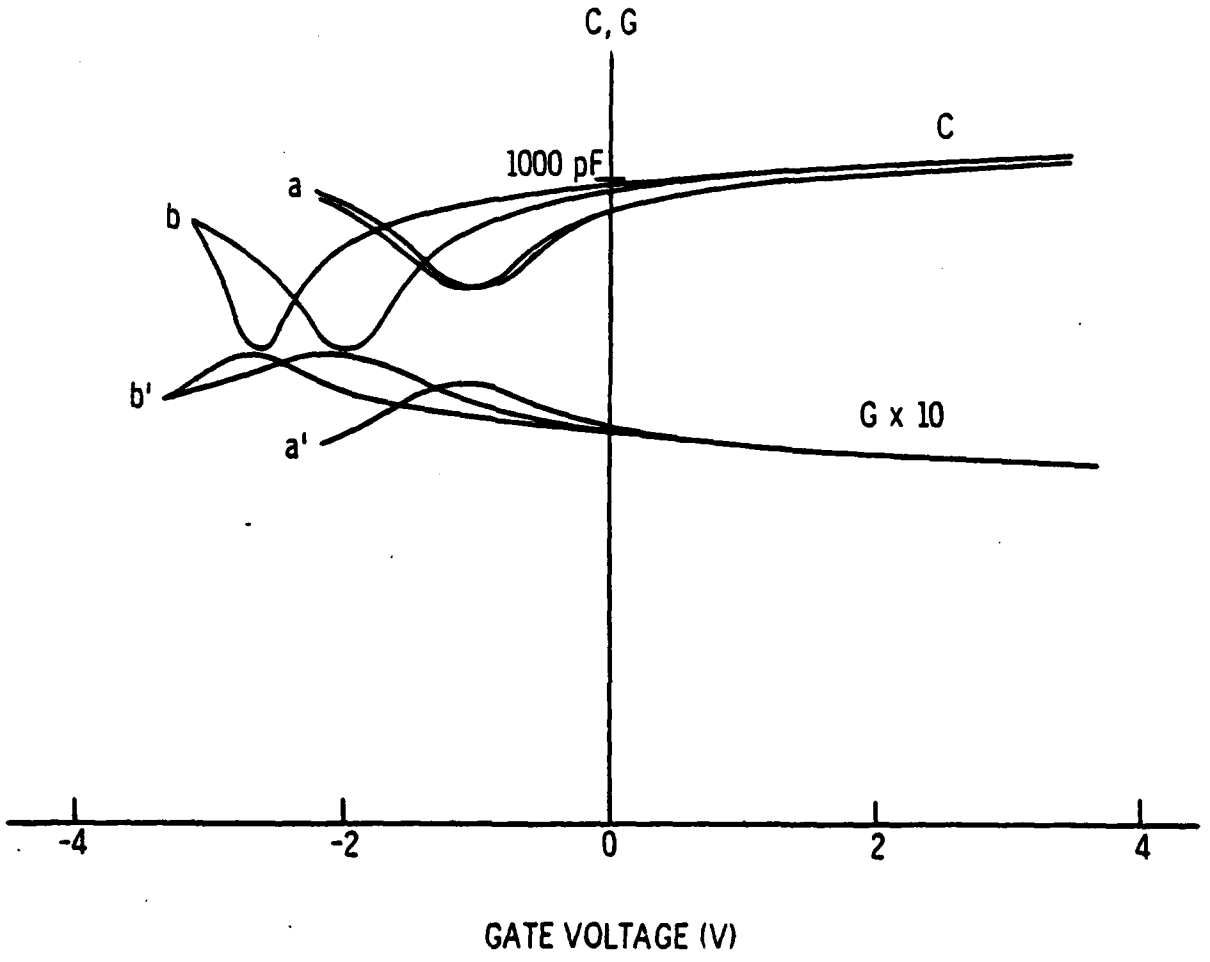

Figure 7. The C-V and G-V curves of an MIS device made with an anodic oxide on $Hg_{0.8}Cd_{0.2}Te$ p = 5.5 x $10^{17}cm^{-3}$ before and after heating at 110°C.

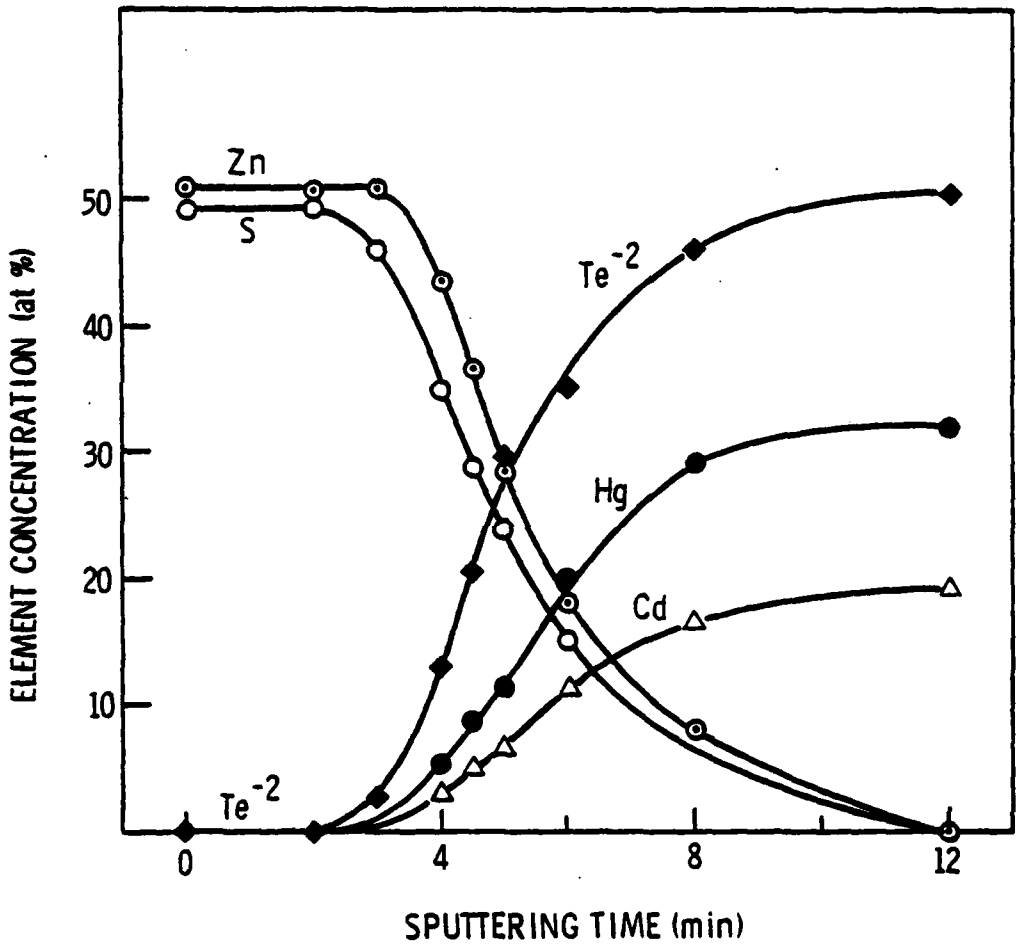

Figure 8. The XPS depth composition profile of an electron beam evaporated film of ZnS on $Hg_{0.8}Cd_{0.2}Te$. The ZnS thickness is 500 Å, determined by a thickness monitor.

ions, thus leading to formation of $ZnS_{1-y}Te_y$. No impurities (e.g., O and C) were detected at the interface. The ratio of Hg/Cd in the semiconductor near the interface was only slightly smaller than the value in the bulk. However, the data was not accurate enough to determine whether there is any significant depletion of cations at the interface.

Because of the strong interaction between the deposited ZnS and the (Hg,Cd)Te substrate, the interface properties are expected to be significantly altered. However, the precise effect on the electrical behavior of devices has yet to be determined.

3.2.2 MIS Measurements

We have investigated the electrical properties of ZnS films deposited by three different techniques:

(i) argon ion sputtering
(ii) electron beam evaporation
(iii) evaporation using a Knudsen cell

ZnS films deposited by argon ion sputtering showed no dependence of the capacitance on the applied voltage. It is suspected that the high energy with which the ZnS impinges on the $Hg_{0.8}Cd_{0.2}Te$ surface causes extensive damage to the semiconductor, thereby producing a large number of electronic surface states. These damage-related surface states prevent the surface potential from being modified by the applied voltages which have to be small enough to avoid electrical breakdown of the ZnS film.

ZnS deposited by electron beam evaporation gave films with much better electrical properties, i.e. control of the surface potential layer, lower loss implying fewer interface states and less hysteresis meaning fewer trapped charges. The C-V curves obtained at two frequencies are shown

in Fig. 9 and further imply that these surfaces, in contrast to those with the anodic oxide, are depleted of majority carriers.

Results for ZnS films obtained by evaporation from a Knudsen cell were electrically unstable and seemed to break down at random potentials. No explanation is available as yet.

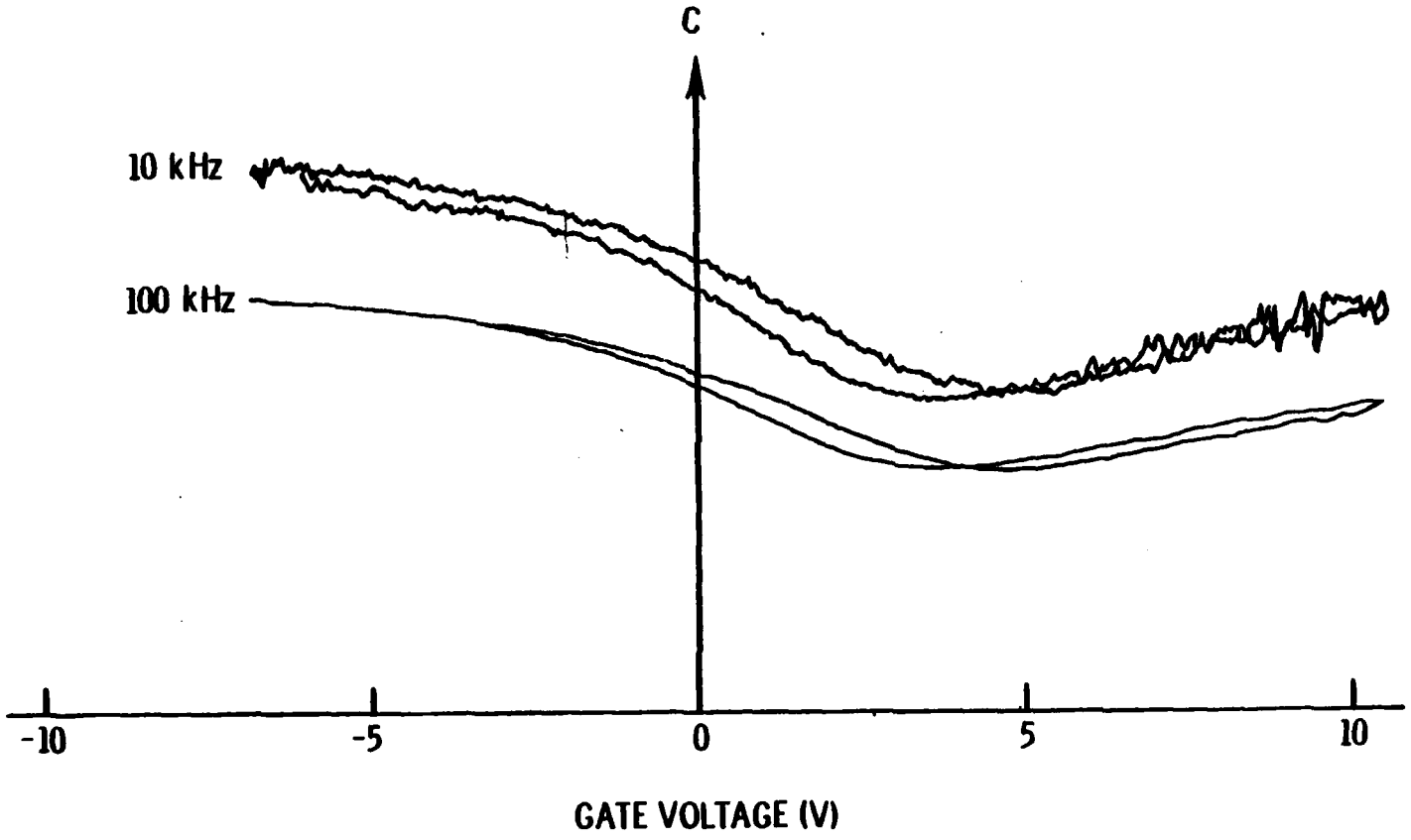

Figure 9. Capacitance as a function of voltage at 77°K for an MIS device made with ZnS deposited by electron beam evaporation as the insulator on p = 5.5×10^{17} cm^{-3} $Hg_{0.8}Cd_{0.2}Te$ at two modulating frequencies. For clarity, the 100 kHz curves are displaced along the capacitance axis from the 10 kHz curves.

4. CONCLUSION AND RECOMMENDATION FOR FUTURE WORK

In summary, the results of our study of the chemical and electrical properties of anodic oxide and ZnS films on $Hg_{0.8}Cd_{0.2}Te$ have the following implications to their use as surface passivants:

(1) The anodic oxide has a large density of trapped charges, possibly due to the presence of unstable HgO in the oxide.

(2) Anodization can cause a substantial depletion of cations in the interface region; as a result, a high density of surface states and other defect states are generated.

(3) The electron beam evaporated ZnS interacts with $Hg_{0.8}Cd_{0.2}Te$ surface, resulting in the formation of a $ZnS_{1-y}Te_y$ interface layer. The nature and the effect of this interfacial compound have yet to be determined.

These results point to a need for improvements in the fabrication of these two insulators, especially in the area of anodization technique where a great number of variables can be manipulated. For instance, by changing the pH of electrolyte and the current density, it is possible to tailor the oxide composition and to minimize cation depletion. Another possible approach is to use the plasma-oxidation technique[10] to grow native oxide. Furthermore, post-anodization treatment, such as annealing process, can also be very important. Chang[12] reported that annealing in different ambient gases produced different effects on the properties of plasma-grown oxides on GaAs. This appears to be an area worth exploration.

A possible improvement may also be achieved by combining both types of insulators, i.e., a thin (<500 Å) anodic oxide film is grown on the surface of (Hg,Cd)Te before deposition of a thick ZnS. The key concept is to optimize the thickness of the anodic oxide so that it is thin enough to reduce the cation depletion at the interfaces significantly but thick enough to prevent any direct interaction between ZnS and (Hg,Cd)Te.

In addition to the improvements in the insulator fabrication techniques, two areas of research are considered to be very important in an extensive effort to relate the interface study to the problem of surface leakage in (Hg,Cd)Te photodiodes. The first one concerns a comprehensive investigation of the material defects near the (Hg,Cd)Te surface using scanning transmission electron microscope and x-ray topography. The second one concerns the use of gate-controlled diode structures which allow one to determine more precisely the origins of the leakage than the MIS measurements. These approaches have been incorporated in a proposed modification to this contract (MML Proposal No. PH79-43R, October 1979).

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6. APPENDIX

6.1 A Simplified Model for Evaluating the Hg Peak Intensity at Oxide/Semiconductor Interface

Because of the curvature and roughness of the sputtered surface, the area probed by the XPS analyzer consists of both oxide region and (Hg,Cd)Te region when the sputtered crater sinks below the interface plane. Let:

A = total area probed by the XPS analyzer;

Z = area of oxide probed;

α = the Hg intensity in the oxide per unit area;

β = the Hg intensity in (Hg,Cd)Te per unit area;

γ = the O intensity in the oxide per unit area.

Here, we assume that α and γ are constant (see Fig. 5), and β is a function of depth. Furthermore, let x = total O intensity, and y = total Hg intensity, then $x = \gamma Z$ (for $0<Z<A$)

$$y = \alpha Z + \beta(A-Z)$$

$$= \frac{\alpha}{\gamma} x + \beta\left(A-\frac{x}{\gamma}\right) \qquad \text{(for } 0<x<1\text{)}$$

Since Z is a function of the sputtered depth, so is x. Consequently, we can regard β as a function of x. The Hg intensity at the interface can be determined by evaluating βA in the limit $x \to 1$. The method is to plot y as a function of x (see Fig. 6), and then draw a line tangent to the curve at x = 1 (line a in Fig. 6). Since its slope is given by $\left.\frac{dy}{dx}\right|_{(x\to 1)} = \frac{\alpha}{\gamma} - \frac{\beta}{\gamma}$, we have $\beta A_{(x\to 1)} = \gamma A$ (-slope of line a) + αA = intersection of line a with the y-axis. Therefore, the Hg intensity is approximately represented by the intersection of line a with y-axis.

7. PUBLICATION

We have submitted a paper entitled, "Oxide and Interface Properties of Anodic Films on $Hg_{1-x}Cd_xTe$" by T. S. Sun, S. P. Buchner and N. E. Byer, to the 7th Physics of Compound Semiconductor Interfaces Conference, Estes Park, Colorad, 29-31 January 1980. The paper has been accepted for presentation in the poster session of that conference and its publication in the Journal of Vacuum Science and Technology will be subjected to reviewing. The abstract of the paper is shown in the next page.

OXIDE AND INTERFACE PROPERTIES OF ANODIC FILMS ON $Hg_{1-x}Cd_xTe$*

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The oxide and interface properties of a 1200 Å anodic film on $Hg_{0.8}Cd_{0.2}Te$ were studied by means of x-ray photoelectron spectroscopy (XPS) and capacitance voltage (C-V) measurements on a metal-oxide-semiconductor (MOS) device. The XPS results showed that the anodic oxide consisted of about 68% TeO_2, 27% CdO, and 6% HgO. A depth profile of the interface region, performed with the aid of Ar^+ sputtering, showed evidence of a 12% depletion of Hg and 6% depletion of Cd in the semiconductor side. These results are inconsistent with the recent model of the same oxide/semiconductor system, proposed by Nemirovsky and Finkman[1]. The C-V curves from MOS measurements exhibited a large hysteresis and a characteristic indicative of a high density of surface states. A tentative interpretation for these results is that the dissociation of HgO into Hg^{+2} and O^{-2} in the anodic film is responsible for the hysteresis, while the cation vacancies in the semiconductor create defect states near the interface. In addition, the results for anodic films on $Hg_{0.7}Cd_{0.3}Te$ and the effects of the electron beam and of ion sputtering on these compounds will be discussed.

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